REMARKS

Status of the Application

Claims 1, 3 and 5-9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yoshikawa (U.S. 5,084,961). Claims 1 and 5-9 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Soga et al. (U.S. Pat. Application Publication No. 2006/0061974). Claims 1-6, 8-12 and 14 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Jairazbhoy et al. (U.S. Pat. Application Publication No. 2002/0000331). Claims 7 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jairazbhoy et al. in view of Soga et al.

By this Amendment, Applicants are amending claim 1.

Claim Rejections - 35 USC § 102

A. Claims 1, 3 and 5-9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yoshikawa (U.S. 5,084,961).

Claim 1 recites, in part, "disposing a plurality of metal bonding film shapes in a pattern directly on a substrate." The Examiner alleges that Yoshikawa discloses all of the elements of claim 1, citing element 16, and FIG. 2b and col. 3, lines 29-41 of Yoshikawa as support. Yoshikawa discloses a method for mounting a circuit on a substrate. The conductive adhesive 16 in FIG. 2A is shown as being disposed *on pectinate electrodes 13*, not on the substrate 11. Because Yoshikawa fails to teach or suggest that the metal bonding film is disposed *directly* on the substrate, amended claim 1 is patentable over the applied art.

Claims 3 and 5-9 are patentable at least by virtue of their dependency from amended claim 1.

B. Claims 1 and 5-9 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Soga et al. (U.S. Pat. Application Publication No. 2006/0061974).

Amended claim 1 recites, in part, "disposing a bonded element above the plurality of metal bonding film shapes and applying heat to the substrate and pressure to the bonded element." The Examiner alleges that Soga teaches all of the elements of claim 1, citing elements 18, 21 and 29, and FIG. 7a and paragraphs [121] and [128]-[130]. Soga discloses a solder foil semiconductor device. FIG. 7a shows Si chips 8, which are attached to a substrate 29 by solder bumps 18. However, while the solder is heated by a resistance heater in order to connect the Si chips to the substrate, Soga fails to teach or suggest that heat is applied to the substrate, and pressure is applied to *the Si chips* (the bonded element), thereby bonding the Si chips to the substrate, as recited in claim 1. Therefore, Soga fails to teach or suggest all of the elements of amended claim 1, and amended claim 1 is patentable over the applied art.

Claims 5-9 are patentable at least by virtue of their dependency from amended claim 1.

C. Claims 1-6, 8-12 and 14 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Jairazbhoy et al. (U.S. Pat. Application Publication No. 2002/0000331).

Amended claim 1 recites, in part, "disposing a plurality of metal bonding film shapes in a pattern directly on a substrate" and "disposing a bonded element above the plurality of metal bonding film shapes and applying heat to the substrate and pressure to the bonded element,

thereby bonding the bonded element to the substrate having the plurality of metal bonding film shapes." The Examiner alleges that Jairazbhoy teaches all of the elements of claim 1, citing elements 16, 80 and FIG. 12b and paragraphs [0036], [0037], [0043] and [0049].

Jairazbhoy discloses a method for making an electric circuit assembly. FIG. 12b shows that solder bumps 16 are disposed on base pads 20, which sit atop a substrate 80. However, Jairazbhoy fails to teach or suggest that the solder bumps are disposed *directly* on the substrate 80. As seen in FIG. 12, base pads are disposed between the solder bumps and the substrate, preventing the solder bumps from being disposed directly on the substrate. Therefore, Jairazbhoy fails to teach disposing a plurality of metal bonding film shapes in a pattern directly on a substrate.

Further, Jairazbhoy fails to teach or suggest applying heat to the substrate and applying pressure to the bonded element. Jairazbhoy teaches that a surface mount electronic component may be soldered to a pair of closely spaced base pads. See paragraph [0036]. Jairazbhoy further teaches that "such a component 93 *rests* generally atop each plurality or cluster of bumps 16." (Emphasis added). See paragraphs [0036] and [0043]. The component resting atop the bumps means implicitly that no pressure is applied to the component. Additionally, heat is applied to the solder bumps, but, Jairazbhoy fails to indicate to which element the heat is applied.

For the reasons outlined above, Jairazbhoy cannot anticipate amended claim 1. Amended claim 1 is patentable over the applied art.

Claims 2-5, 8-12 and 14 are patentable at least by virtue of their dependency from amended claim 1.

Claim Rejections - 35 USC § 103

Claims 7 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jairazbhoy et al. in view of Soga et al.

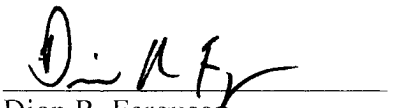
Claims 7 and 13 are dependent from amended claim 1. Therefore, because Jairazbhoy fails to teach or suggest all of the elements of claim 1, and because Soga fails to cure the defects noted in Jairazbhoy with respect to amended claim 1, claims 7 and 13 are patentable at least by virtue of their dependency.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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